Integrated Circuit Systems, Inc.

ICS853014

LOW SKEW, 1-TO-5 2.5V/3.3V DIFFERENTIAL-TO-LVPECL/ECL FANOUT BUFFER

GENERAL DESCRIPTION

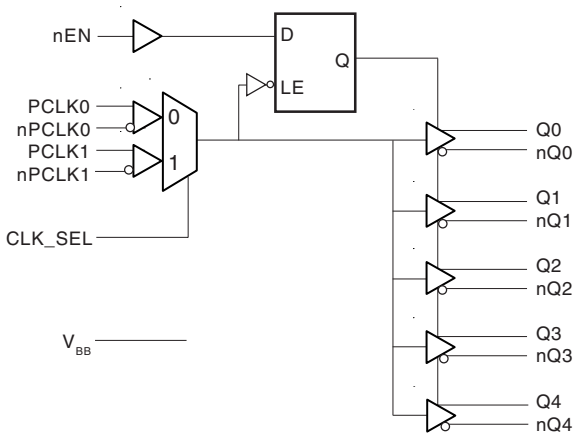
The ICS853014 is a low skew, high performance 1-to-5, 2.5V/3.3V Differential-to-LVPECL/ECL Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS853014 has two selectable clock inputs.

Guaranteed output and part-to-part skew characteristics make the ICS853014 ideal for those applications demanding well defined performance and repeatability.

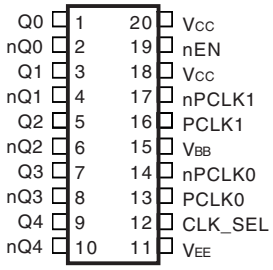
FEATURES

- 5 differential LVPECL/ECL outputs
- 2 selectable differential LVPECL clock inputs
- PCLKx, nPCLKx pairs can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Maximum output frequency: > 2GHz
- Output skew: 13ps (typical)
- Part-to-part skew: 60ps (typical)
- Propagation delay: 460ps (typical)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Lead-Free package fully RoHS compliant

BLOCK DIAGRAM



PIN ASSIGNMENT



ICS853014
20-Lead TSSOP
6.5mm x 4.4mm x 0.92mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL / ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL / ECL interface levels.
5, 6	Q2, nQ2	Output		Differential output pair. LVPECL / ECL interface levels.
7, 8	Q3, nQ3	Output		Differential output pair. LVPECL / ECL interface levels.
9, 10	Q4, nQ4	Output		Differential output pair. LVPECL / ECL interface levels.
11	V_{EE}	Power		Negative supply pin.
12	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects CLK1, nCLK1 inputs. When LOW, selects CLK0, nCLK0 inputs. LVTTL / LVCMOS interface levels.
13	PCLK0	Input	Pulldown	Non-inverting differential LVPECL clock input.
14	nPCLK0	Input		Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
15	V_{BB}	Output		Bias voltage.
16	PCLK1	Input	Pulldown	Non-inverting differential LVPECL clock input.
17	nPCLK1	Input		Inverting differential LVPECL clock input. V_{CC}/2 default when left floating.
18, 20	V_{CC}	Power		Positive supply pins.
19	nEN	Input	Pulldown	Synchronizing clock enable. When LOW, clock outputs follow clock input. When HIGH, Q outputs are forced low, nQ outputs are forced high. LVTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ
$R_{VCC/2}$	Pullup/Pulldown Resistors			50		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs			Outputs	
nEN	**CLK_SEL**	**Selected Source**	**Q0:Q4**	**nQ0:nQ4**
1	0	PCLK0, nPCLK0	Disabled; LOW	Disabled; HIGH
1	1	PCLK1, nPCLK1	Disabled; LOW	Disabled; HIGH
0	0	PCLK0, nPCLK0	Enabled	Enabled
0	1	PCLK1, nPCLK1	Enabled	Enabled

After nEN switches, the clock outputs are disabled or enabled following a falling input clock edge as shown in *Figure 1.* In the active mode, the state of the outputs are a function of the PCLK0, nPCLK0 and PCLK1, nPCLK1 inputs as described in *Table 3B.*

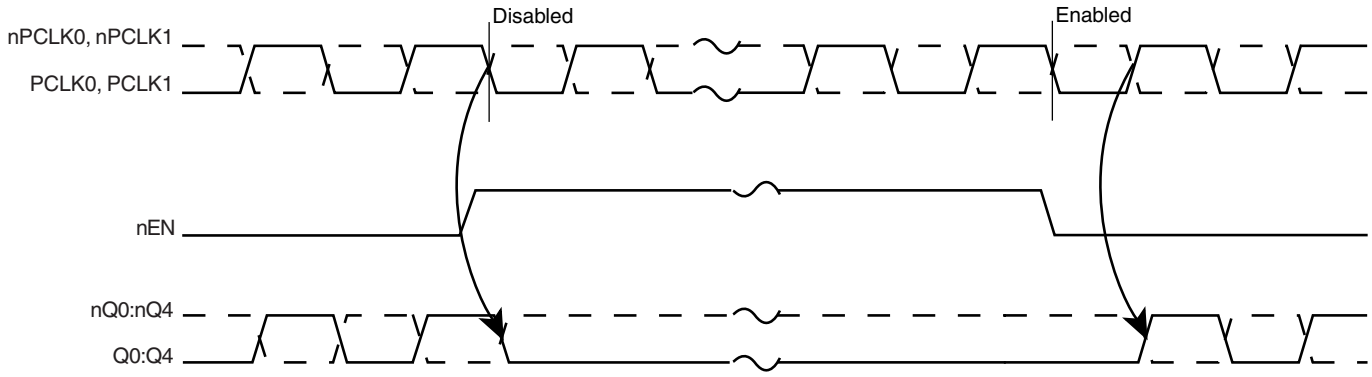


FIGURE 1. nEN TIMING DIAGRAM

TABLE 3B. CLOCK INPUT FUNCTION TABLE

Inputs		Outputs		Input to Output Mode	Polarity
PCLK0 or PCLK1	**nPCLK0 or nPCLK1**	**Q0:Q4**	**nQ0:nQ4**		
0	1	LOW	HIGH	Differential to Differential	Non Inverting
1	0	HIGH	LOW	Differential to Differential	Non Inverting
0	Biased; NOTE 1	LOW	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	HIGH	LOW	Single Ended to Differential	Non Inverting
Biased; NOTE 1	0	HIGH	LOW	Single Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single Ended to Differential	Inverting

NOTE 1: Please refer to the Application Information section, "Wiring the Differential Input to Accept Single Ended Levels".

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} - 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
V_{BB} Sing/Source, I_{BB}	± 0.5mA
Operating Temperature Range, TA	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient)	73.2°C/W (0 lfpm)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V; V_{EE} = 0V

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				75	mA

TABLE 4B. DC CHARACTERISTICS, V_{CC} = 3.3V, V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.375	2.22	2.295	2.365	V
V_{OL}	Output Low Voltage; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{IH}	Input High Voltage(Single-Ended)		2.075		2.36	2.075		2.36	2.075		2.36	V
V_{IL}	Input Low Voltage(Single-Ended)		1.43		1.765	1.43		1.765	1.43		1.765	V
V_{BB}	Output Voltage Reference; NOTE 2		1.86		1.98	1.86		1.98	1.86		1.98	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	D0, D1, D2, D3 nD0, nD1,n D2, nD3			150			150			150	µA
I_{IL}	Input Low Current	D0, D1, D2, D3	-10			-10			-10			µA
		nD0, nD1,n D2, nD3	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPLCK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 4C. LVPECL DC CHARACTERISTICS, V_{CC} = 2.5V; V_{EE} = 0V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.42	1.495	1.565	V
V_{OL}	Output Low Voltage; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{IH}	Input High Voltage(Single-Ended)		1.275		1.56	1.275		1.56	1.275		-0.83	V
V_{IL}	Input Low Voltage(Single-Ended)		0.63		0.965	0.63		0.965	0.63		0.965	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	-10			-10			-10			µA
		nPCLK0, nPCLK1	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 4D. ECL DC CHARACTERISTICS, V_{CC} = 0V; V_{EE} = -5.25V TO -2.375V

Symbol	Parameter		-40°C			25°C			85°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Voltage; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.08	-1.005	-0.935	V
V_{OL}	Output Low Voltage; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{IH}	Input High Voltage(Single-Ended)		-1.225		-0.94	-1.225		-0.94	-1.225		-0.94	V
V_{IL}	Input Low Voltage(Single-Ended)		-1.87		-1.535	-1.87		-1.535	-1.87		-1.535	V
V_{BB}	Output Voltage Reference; NOTE 2		-1.44		-1.32	-1.44		-1.32	-1.44		-1.32	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 3, 4		V_{EE}+1.2V		0	V_{EE}+1.2V		0	V_{EE}+1.2V		0	V
I_{IH}	Input High Current	PCLK0, PCLK1 nPCLK0, nPCLK1			150			150			150	µA
I_{IL}	Input Low Current	PCLK0, PCLK1	-10			-10			-10			µA
		nPCLK0, nPCLK1	-150			-150			-150			µA

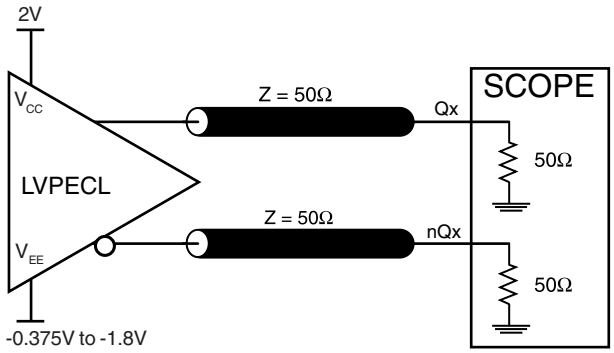
Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} - 2V.
NOTE 2: Single-ended input operation is limited. $V_{CC} \geq$ 3V in LVPECL mode.
NOTE 3: Common mode voltage is defined as V_{IH}.
NOTE 4: For single-ended applications, the maximum input voltage for PCLK0, nPCLK0 and PCLK1, nPCLK1 is V_{CC} + 0.3V.

TABLE 5. AC CHARACTERISTICS, V_{CC} = 2.375V TO 3.8V, T_A = -40°C TO 85°C

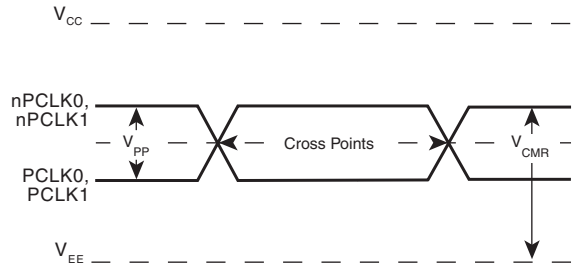
Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency		>2			>2			>2		GHz
t_{PD}	Propagation Delay; NOTE 1	355	440	525	376	460	550	400	500	595	ps
*t*sk(o)	Output Skew; NOTE 2, 5		13	25		13	25		12	25	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 5			105			105			130	ps
V_{PP}	Peak-to-Peak Input Voltage; NOTE 4	150	800	1800	150	800	1800	150	800	1800	mV
t_R/t_F	Output Rise/Fall Time 20% to 80%	90	150	210	90	150	210	90	150	210	ps
t_S	Clock Enable Setup Time	100	50		100	50		100	50		ps
t_H	Clock Enable Hold Time	200	140		200	140		200	140		ps

All parameters tested ≤ 1GHz unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: The VCMR and V_{PP} levels should be such that input low voltage never goes below V_{EE}.
NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

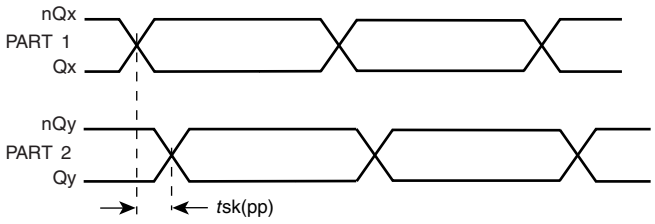
PARAMETER MEASUREMENT INFORMATION



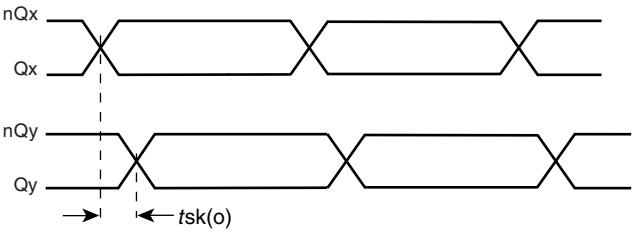
OUTPUT LOAD AC TEST CIRCUIT



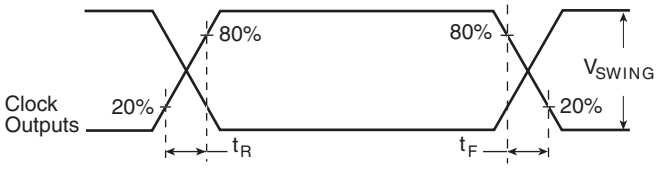
DIFFERENTIAL INPUT LEVEL



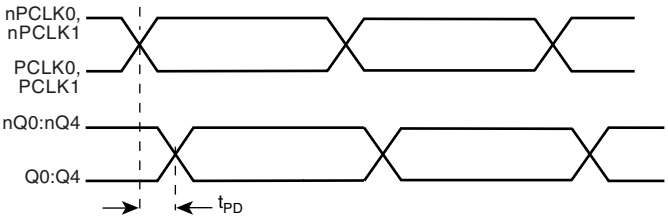
PART-TO-PART SKEW



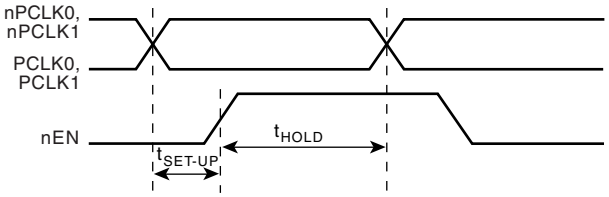
OUTPUT SKEW



OUTPUT RISE/FALL TIME



PROPAGATION DELAY



SETUP AND HOLD TIME

APPLICATION INFORMATION

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows an example of the differential input that can be wired to accept single ended levels. The reference voltage level V_{BB} generated from the device is connected to the negative input. The C1 capacitor should be located as close as possible to the input pin.

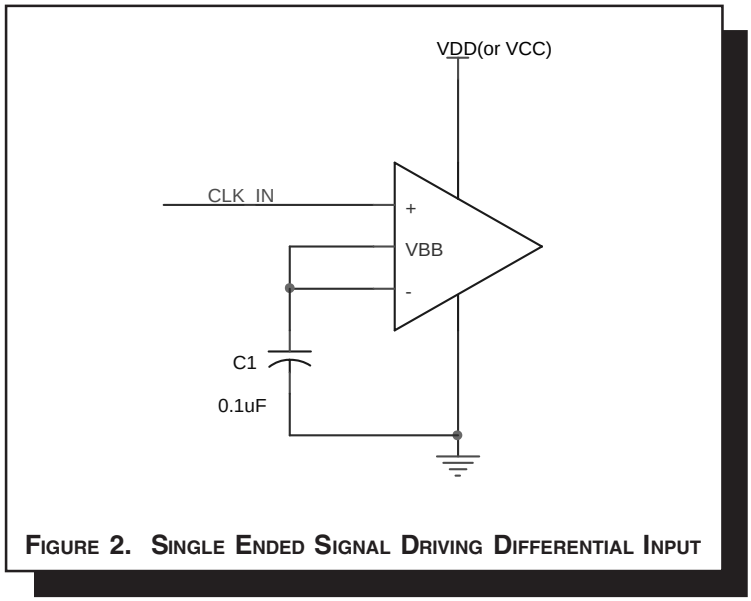


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

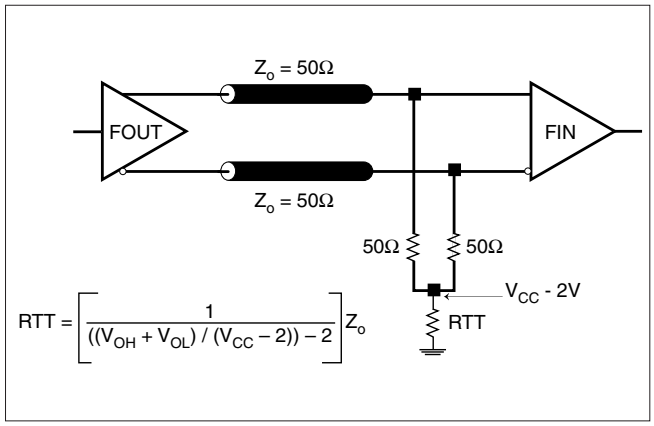


FIGURE 3A. LVPECL OUTPUT TERMINATION

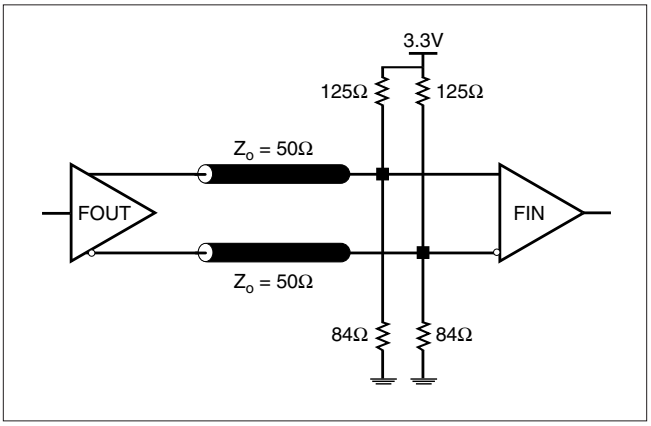


FIGURE 3B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} - 2V. For V_{CC} = 2.5V, the V_{CC} - 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

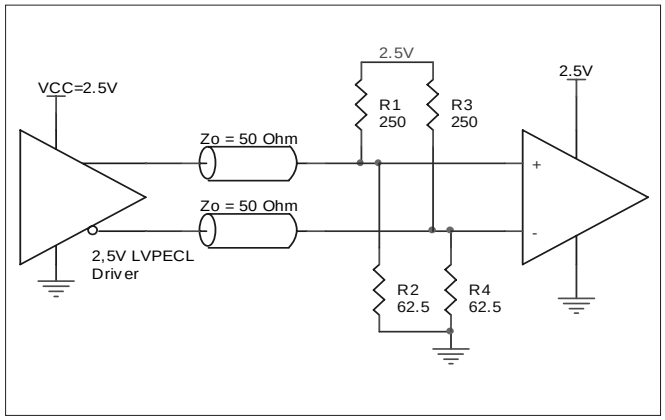


FIGURE 4A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

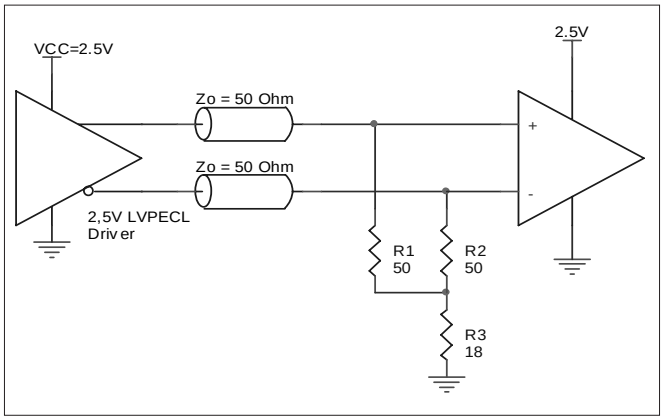


FIGURE 4B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

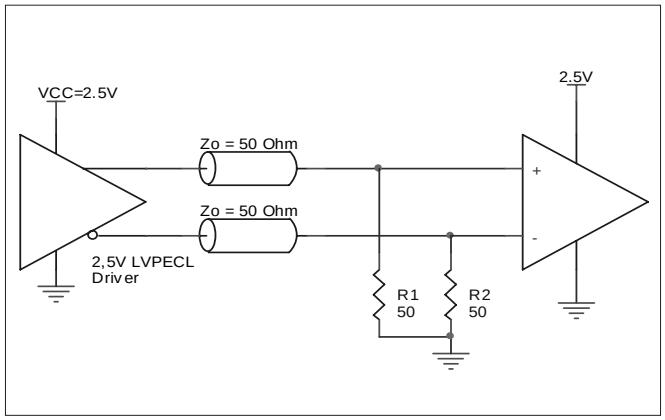


FIGURE 4C. 2.5V LVPECL TERMINATION EXAMPLE

LVPECL CLOCK INPUT INTERFACE

The PCLKx /nPCLKx accepts LVPECL, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 5A to 5E* show interface examples for the HiPerClockS PCLKx/nPCLKx input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

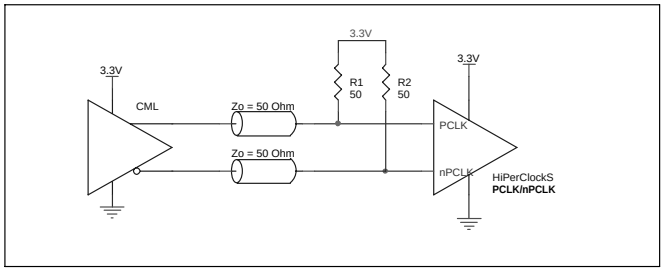


FIGURE 5A. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A CML DRIVER

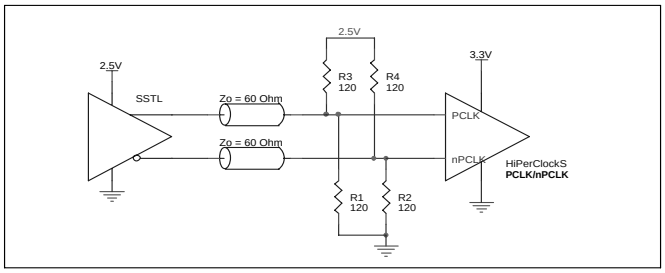


FIGURE 5B. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY AN SSTL DRIVER

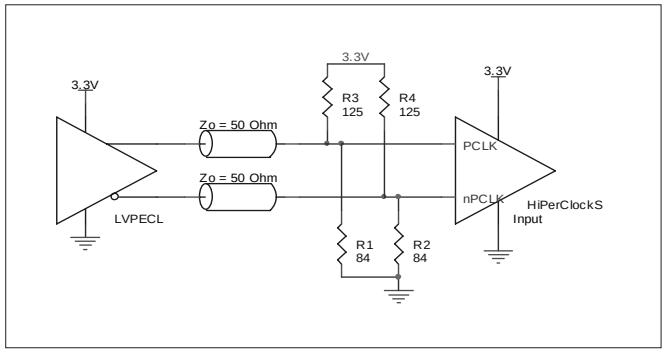


FIGURE 5C. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

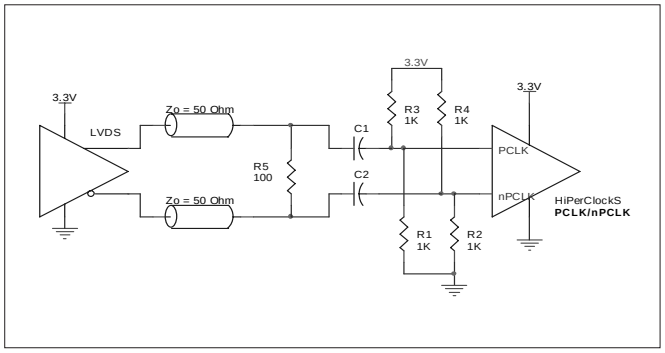


FIGURE 5D. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

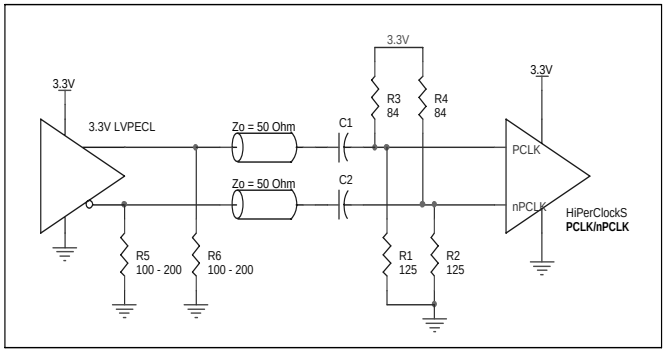


FIGURE 5E. HIPERCLOCKS PCLK/nPCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER WITH AC COUPLE

SCHEMATIC EXAMPLE

This application note provides general design guide using ICS853014 LVPECL buffer. *Figure 6* shows a schematic example of the ICS853014 LVPECL clock buffer. In this example, the input is driven by an LVPECL driver. CLK_SEL is set at logic high to select PCLK1/nPCLK1 input.

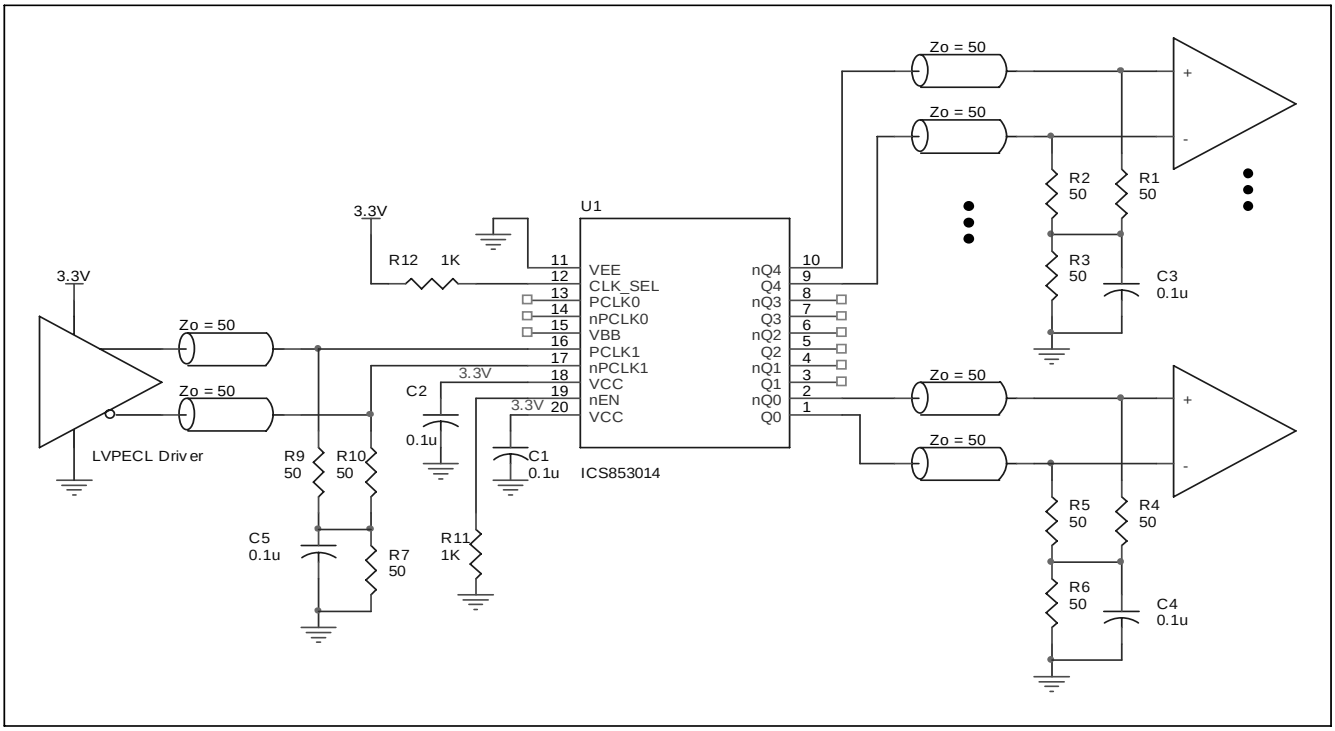


FIGURE 6. EXAMPLE ICS853014 LVPECL CLOCK OUTPUT BUFFER SCHEMATIC

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS853014.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS853014 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.8V * 75mA = **285mW**
- Power $(outputs)_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 5 * 30.94mW = **154.7mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 285mW + 154.7mW = **439.7mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.440W * 66.6°C/W = 114.3°C. This is well below the limit of 125°C

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 20-PIN TSSOP, FORCED CONVECTION

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

LVPECL output driver circuit and termination are shown in *Figure 7.*

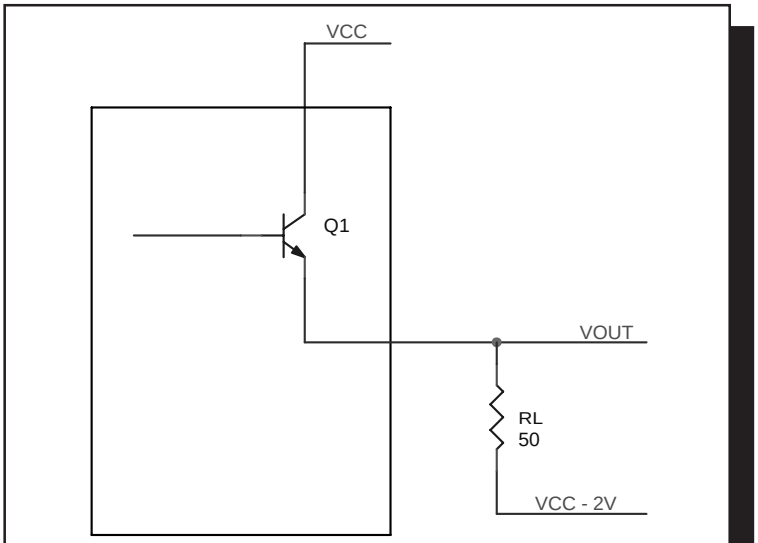


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} - 0.935V}$

  $(V_{CC\_MAX} - V_{OH\_MAX}) = \mathbf{0.935V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} - 1.67V}$

  $(V_{CC\_MAX} - V_{OL\_MAX}) = \mathbf{1.67V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} - 2V))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CC\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.67V)/50\Omega] * 1.67V =$ **11.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 20 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for ICS853014 is: 373

Pin compatible with MC100LVEP14 and SY100EP14U

PACKAGE OUTLINE - G SUFFIX FOR 20 LEAD TSSOP

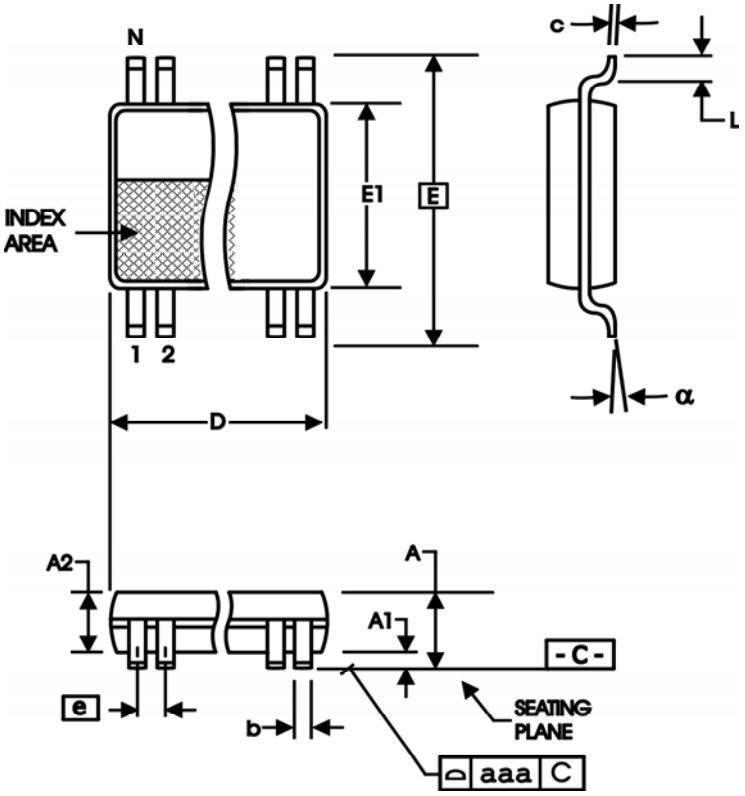


TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853014BG	ICS853014BG	20 lead TSSOP	tube	-40°C to 85°C
ICS853014BGT	ICS853014BG	20 lead TSSOP	2500 tape & reel	-40°C to 85°C
ICS853014BGLF	ICS853014BGL	20 lead "Lead-Free" TSSOP	tube	-40°C to 85°C
ICS853014BGLFT	ICS853014BGL	20 lead "Lead-Free" TSSOP	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
B	T4B	pg. 4	• 3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	9/10/03
	T4C	pg. 5	• 3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	
	T4D	pg. 5	• 3.3V LVPECL table - V_{OH} values changed @ 85° to 2.22V min. and 2.295V typical from 2.295V min. and 2.33V typical.	
		pg. 8	• Revised LVPECL Output Termination drawings.	
		pg. 10	• Revised Figure 5D.	
C	T4B - T4D	pgs. 4-5	• LVPECL & ECL tables - deleted V_{PP} row.	3/18/04
		pg. 6	• AC Table - added V_{PP} row and changed max. value from 1200mV to 1800mV.	
C		1	Features Section - added Lead-Free bullet.	5/13/05
	T9	16	Ordering Information Table - added Lead-Free part number.	